WHAT IS CLAIMED:

1. A method of forming a Spin-On-Glass (SOG) layer in an integrated circuit, the method comprising:

forming an SOG layer on an integrated circuit substrate;

performing a first curing process on the SOG layer;

removing less than all of the SOG layer from the integrated circuit substrate through a mask pattern on the SOG layer to provide a remaining portion of the SOG layer on the integrated circuit substrate;

performing a second curing process on the remaining portion of the SOG layer; and

removing the remaining portion of the SOG layer to expose the integrated circuit substrate.

2. A method according to Claim 1 wherein said step of removing comprises:

etching the SOG layer through the mask pattern to form a recess in the SOG layer, wherein the recess has a bottom formed of the SOG layer that is spaced-apart from the integrated circuit substrate by a thickness of the bottom.

3. A method according to Claim 2 wherein etching is performed using a C-F based gas, CO gas, O_2 gas and an inert gas as etching gas, reaction gas and atmospheric gas, respectively.

4. A method according to Claim 2 wherein etching is performed at an RF power in a range between about 1000 Watts and about 2000 Watts at a pressure in a range between about 10 mTorr and about 100 mTorr and a temperature in a range between about 0 °C and about 60 °C for a time in a range between about 20 second and about 50 seconds.

5. A method according to Claim 2 wherein etching is performed using at an RF power in a range between about 1000 Watts and about 2000 Watts at a pressure in a range between about 10 mTorr and about 100 mTorr and a temperature in a range

between about 0°C and about 60 °C for a time in a range between about 5 second and about 30 seconds.

6. A method according to Claim 2 wherein forming an SOG layer comprises:

forming a stopper layer on the integrated circuit substrate on which a predetermined pattern has been formed; and

forming the SOG layer on the stopper layer, wherein the stopper layer is etched using the mask pattern after etching the SOG layer.

7. A method according to Claim 6 wherein the stopper layer comprises a silicon nitride layer (Si_3N_4), an aluminum oxide layer Al_2O_3, an aluminum nitride layer AlN, a titanium nitride layer TiN or a tantalum nitride layer (TaN).

8. A method according to Claim 2 wherein said step of etching the bottom is followed by:

cleaning the integrated circuit substrate; and

forming a conductive layer in the recess on the integrated circuit substrate.

9. A method according to Claim 1 wherein said step of performing the first curing process comprises performing the first curing process at a temperature in a range between about 600 °C and about 800 °C for a time in a range between about 20 minutes and about 2 hours.

10. A method according to Claim 1 wherein said step of performing the second curing process comprises performing the second curing process at a temperature in a range of between about 400 °C and about 800 °C for a time in a range of between about 10 minutes and about 1 hour.

11. A method according to Claim 1 wherein the first and second curing processes are performed using H_2O, O_2, N_2, H_2, NO_2 or a mixture of these gases as an atmospheric gas.

12. A method according to Claim 1 wherein the remaining portion has a thickness that is adequate to prevent oxidation of the integrated circuit substrate during the second curing process.

13. A method according to Claim 12 wherein the thickness is in a range between about 300 Ångstroms and about 500 Ångstroms.

14. A method according to Claim 1 wherein the mask pattern is formed of a polysilicon layer, an aluminum oxide layer (Al_2O_3), an aluminum nitride layer (AlN) or a silicon nitride layer (Si_3N_4).